What Is Claimed Is:

1. A one-time programing memory element, capable of being manufactured in a 0.13μm or below CMOS technology, comprising:

a capacitor having an oxide layer capable of passing direct gate tunneling current; and

a switch having a voltage tolerance higher than that of said capacitor;

wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage across said oxide layer via said switch to cause direct gate tunneling current to rupture said oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

2. The one-time programing memory element according to claim 1, wherein said oxide layer is approximately 20Å thick.

3. The one-time programing memory element according to claim 1, wherein said capacitor comprises a field effect transistor having source and drain regions coupled to ground, a gate coupled to said switch and a gate dielectric forming said oxide layer.

4. The one-time programing memory element according to claim 3, wherein said field effect transistor has a deep N-well design.

5. The one-time programing memory element according to claim 1, wherein said switch comprises a 5volt tolerant switch having plural 2.5 volt transistors with gate oxide layers that are thicker than said oxide layer.

6. The one-time programing memory element according to claim 1, further comprising a sensing circuit to sense whether said capacitor is programmed.

7. The one-time programing memory element according to claim 1, wherein a charge pump is not required to program said anti-fuse.

8. A process, compatible with 0.13μm or below CMOS technology, for making a one-time programing memory element, comprising the steps of:

forming a capacitor having an oxide layer capable of passing direct gate tunneling current; and

forming a switch having a voltage tolerance higher than that of said capacitor;

wherein said capacitor is one-time programmable as an anti-fuse, without a charge pump, by application of a voltage across said oxide layer via said switch to cause direct gate tunneling current to rupture said oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

9. The process according to claim 8, wherein said oxide layer is formed to a thickness of approximately 20Å thick.

10. The according to claim 8, wherein said forming a capacitor step comprises forming a field effect transistor having source and drain regions coupled to ground, a gate coupled to said switch and a gate dielectric forming said oxide layer.

11. The process according to claim 10, wherein said forming a field effect transistor step further includes forming a deep N-well.

12. The process according to claim 8, wherein said forming switch step comprises forming a 5volt tolerance switch having plural 2.5 volt transistors with gate oxide layers that are thicker than said oxide layer.

13. The process according to claim 8, further comprising the step of forming a sensing circuit to sense whether said capacitor is programmed.

14. The process according to claim 8, wherein said process does not require forming a charge pump to program said anti-fuse.